SPECIFICATION

Please amend the specification by making the following amendments:

Please substitute the following for the second full paragraph on Page 6:

A chip receiver 206 is connected to the data bus 200 for receiving the bus_clk. The chip receiver 206 is also connected to a deskew circuit 208. The deskew circuit 208 ~~adjust~~ adjusts delay differences between different bit lines. Additionally, the deskew circuit 208 does the job of splitting the bus_clk into c1-c4 clock signals. Alternatively, a clock generator ([[now]] not shown) could be used to split the bus_clk into c1-c4 clock signals. Preferably, the c1 and c3 clock signals are the deskewed version of the bus_clk. The c2 and c4 clock signals are the inversions of the c1 and c3 clock signals, respectively.

Please substitute the following for the paragraph beginning on line 21 on Page 6:

The deskew circuit 204 is connected to four select circuits 210, 212, 214, and 216 for sending data to the four select circuits 210, 212, 214, and 216. The select circuits 210, 212, 214, and 216 are connected to latches 218, 220, 222, and 224, respectively, for sending data to the respective latches 218, 220, 222, and 224, and for receiving feedback data from the respective latches 218, 220, 222, and 224. The select circuits 210, 212, 214, and 216 are controlled by control signals g1, g2, g3, and g4, respectively. The select circuits 210, 212, 214, and 216 are configured to output the data received from the deskew circuit [[201]] 204 when the control signals are asserted, and are configured to output the feedback data received from the latches 218, 220, 222, and 224 when the control signals are deasserted. The deskew circuit 208 is connected to the latches 218, 220, 222, and 224 for clocking them using the c1, c2, c3, and c4 signals, respectively. As mentioned above, the c1, c2, c3, and c4 signals are derived from the bus_clk. The latches 218, 220, 222, and 224 each may be replaced with a register (not shown) comprising a N number of latches (not shown). In that case, the data received by the interfacing circuit 144 is N bits.